AMENDMENTS TO THE CLAIMS

Claims 1 – 36. (canceled)

37. (original) A method of reading a resistive memory device comprising a plurality of stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns, said method comprising:

decoding a selected memory cell address as a column select signal, a row select signal, and a layer select signal;

using said layer select signal to select one of said layers for a read operation;

using said row select signal to select a row of memory cells of said selected one layer; and

using said column select signal to select the same column of memory cells in each of said layers by turning on an access transistors coupled to said same columns.

38. (original) A method as in claim 37, wherein said resistive memory cells are MRAM memory cells.

39. (original) A method as in claim 38 further comprising sensing a resistance value of a selected memory cell with a sense amplifier coupled to said access transistor.

Claims 40 – 61. (canceled)